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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

09/818,911

03/28/2001

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NE203-US

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7590

05/27/2004

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EXAMINER

JOHNSON, TIMOTHY M

ART UNIT

PAPER NUMBER

2625

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/818,911

Applicant(s)

KATO, SATOSHI

m

Examiner

Timothy M Johnson

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed April 20, 2004 have been approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Nagano, 5,687,003.

For claim 1, an image sensing apparatus comprising: an image quality mode setting block for setting only one of a plurality of image quality modes is provided by Nagano in at least Fig. 1, block 52, and the last full paragraph in c. 4; a solid state image sensing element for converting an optical image into an electric analog signal is provided by Nagano also in at least the last full paragraph in c. 4; and an A/D conversion block for converting the analog signal output from the solid state image sensing element into a digital signal with a quantization bit count corresponding only to the one image quality mode set by the image quality mode setting block also in the last full paragraph in c. 4, the first full paragraph in c. 5, and the third full paragraph in c. 6, as there is only one quality mode set at a time for selection of a corresponding bit count, of which bit count directly corresponds to only one of the A/D converters which convert

to digital with a quantization bit count corresponding only to the one quality mode.

For claim 4, the image sensing apparatus as claimed in claim 1, wherein a higher image quality mode corresponds to a greater bit count and a lower image quality mode corresponds to a smaller bit count is provided by Nagano in at least the last full paragraph in c. 4, e.g. 12 bit and 8 bit counts.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 14-17 and 24 are rejected under 35 U.S.C. § 102(e) as being anticipated by Johnson et al., 6,686,957.

For claim 14, an image quality mode setting block for setting one of a plurality of image quality modes is provided by Johnson in at least the abstract, Figs. 1-2, 4B, 5A, 7A, 7B, the paragraph bridging cols. 1-2, the last full paragraph in c. 4, the paragraph bridging cols. 4-5, the paragraph bridging cols. 5-6, and c. 7, line 60 – c. 8, line 62, where Johnson clearly teaches control of the A/D converter (or ADC) in different quality modes. A solid state image sensing element for converting an optical image into an

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electric analog signal is provided by Johnson in at least Fig. 1, the abstract, the last two full paragraphs in c. 3, and in the paragraph bridging cols. 1-2, where the system is clearly a camera system with a solid state image sensor. An A/D conversion block for converting the analog signal from the solid state image sensing element into a digital signal, the A/D conversion block having a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes, wherein the A/D conversion block is responsive to the image quality mode set by the image quality mode setting block to enable the quantization bit count corresponding to the set image quality mode and disables other quantization bit counts is provided by Johnson in at least the abstract, Figs. 1-2, 4B, 5A, 7A, 7B, the paragraph bridging cols. 1-2, the last full paragraph in c. 4, the paragraph bridging cols. 4-5, the paragraph bridging cols. 5-6, and c. 7, line 60 – c. 8, line 62, where Johnson clearly teaches control of the A/D converter (or ADC) in different quality modes corresponding to a plurality of quantization bit counts.

For claim 15, the image sensing apparatus as claimed in claim 14, wherein the A/D conversion block comprises an A/D converter having a plurality of quantization bit counts corresponding respectively to the image quality modes, wherein the image quality mode setting block selects one of the quantization bit counts is provided by Johnson in at least the abstract, Figs. 1-2, 4B, 5A, 7A, 7B, the paragraph bridging cols. 1-2, the last full paragraph in c. 4, the paragraph bridging cols. 4-5, the paragraph bridging cols. 5-6, and c. 7, line 60 – c. 8, line 62.

For claim 16, the image sensing apparatus as claimed in claim 14, wherein a higher image quality mode corresponds to a greater bit count and a lower image quality mode corresponds to a smaller bit count is provided by Johnson in at least the abstract, Figs. 1-2, 4B, 5A, 7A, 7B, the paragraph bridging cols. 1-2, the last full paragraph in c. 4, the paragraph bridging cols. 4-5, the paragraph bridging cols. 5-6, and c. 7, line 60 – c. 8, line 62, e.g. where 6 bits vs. higher bits corresponds to a lower resolution level, and thus lower quality.

For claim 17, the image sensing apparatus as claimed in claim 14, further comprising a DSP block for performing image processing of the digital signal from the A/D conversion block is provided by Johnson in at least Fig. 1 and the paragraph bridging cols. 1-2, where a DSP for the image is explicitly provided.

For claim 24, the image sensing apparatus as claimed in claim 14, wherein the image sensing apparatus comprises an electronic still camera is provided by Johnson in at least the abstract, the paragraph bridging cols. 1-2, and the third full paragraph in c. 8.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of either JP08298601, Koji et al., as cited in the IDS, or JP401176119, Murakami.

For claim 2, the image sensing apparatus as claimed in claim 1, wherein the A/D conversion block comprises an A/D converter for selecting one of a plurality of quantization bit counts corresponding to the image quality mode is considered provided by Nagano where cited above, and by at least blocks 42, 51, and 53, where a specific bit count is clearly selected. While an A/D converter for selecting one of a quantization bit counts is considered provided by Nagano by at least blocks 51-53 and 42, because a quantization bit count is selected for an A/D converter, and an A/D converter is selected, either JP08298601 or JP401176119 provides for the same in at least the abstract of both. It would've been obvious to one having ordinary skill in the art at the time the invention was made to select one of a plurality of quantization bit counts corresponding to a mode for an A/D converter, since JP401176119 provides for reducing the power consumption, and JP08298601 provides for avoiding error and deterioration.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of Tani, EP 760,514 A2.

For claim 3, the image sensing apparatus as claimed in claim 1, wherein the A/D conversion block comprises a plurality of A/D converters having different quantization bit counts, and an A/D converter selection block for selecting one of the A/D converters corresponding to the image quality mode set by the image quality mode setting block is clearly provided by Nagano in at least Fig. 1 and as noted above for claim 1 with respect to Nagano. Selecting one of the A/D converters to be activated and the other A/D converters to be maintained inactive is provided by at least the data selector 53 in Fig. 1 of Nagano. However, in light of the Applicant's specification, it is understood that inactive means un-powered in the narrow sense, which is not explicitly provided by Nagano. However, keeping some A/D converters actively powered and others inactively powered is conventional and well known, and is provided by Tani in at least the abstract, the last full paragraph in c. 2, and the paragraph bridging cols. 2-3. This idea can clearly be used with selection of A/D converters of Nagano for selecting an A/D converter by applying power and not selecting other A/D converters by not supplying power, since only one of the A/D converters of Nagano is used at any one time, which is in accordance with Applicant's specification. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use the idea of selecting an A/D converter by applying power and not selecting other A/D converters by not supplying power, since Tani teaches the advantages of, inter alia, "saving ADC power consumption" – same exact purpose of Applicant's specification.

9. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Nagano, 5,687,003, as applied to claims 1 and 4 above, and in view of Hasegawa et al., 5,384,645.

For claims 5 and 6, the image sensing apparatus as claimed in claim 1, further comprising a digital signal processing DSP block for performing image processing of the digital signal output from the AD conversion block, the DSP block having a quantization bit count corresponding to the image quality mode set by the image quality mode setting block, and wherein the digital signal processing block sets a corresponding quantization bit count when an image quality mode is set by the image quality mode setting block is almost implicit with Nagano, since Nagano provides for an image reader in the well known image processing systems as noted in c. 1, lines 10-14, which very commonly provide for at least one image processing function, and since such an image processor gets its input from the image sensing system of Nagao, such system would operate in accordance with the quantization bit count set by Nagano. In any case, Hasegawa explicitly teaches this in at least the second full paragraph in c. 3. Adapting the DSP, i.e. image processing, of Hasegawa with a different quantization bit count is exactly what Hasegawa teaches, and image processing is the next stage in the processing of Nagao, where Nagao outputs different quantization bit counts based on modes. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use a DSP for different quantization bit counts, since Hasegawa provides for at least the advantages of a decrease in circuitry heat and therefore a reduction in power consumption as well, improvement in processing speed, and without changing memory to process image data.

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10. Claims 7, 9, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, as applied to claims 5-6 above, and further in view of Nagai, 2001/0010561.

For claim 7, the image sensing apparatus as claimed in claim 5, further comprising a data thinning block for thinning the output signal from the digital signal processing DSP block is not explicitly provided by Nagano, but is conventional and well known, and is provided by Nagai in at least paragraphs 25-26 on page 2, which is provided after or to the output of the digital signal processing as claimed. It would've been obvious to one having ordinary skill in the art at the time the invention was made to thin the output of a DSP in processing, since this provides for at least fast processing.

For claims 9 and 13, the image sensing apparatus as claimed in claim 5, further comprising an image storage block for storing the output signal from the digital signal processing block as image data; and further comprising an image display block for displaying an image according to the output signal from the digital signal processing block, the image display block selecting whether to display the image during storage of image data in the image storage block is not explicitly provided by Nagano and Hasegawa, but is conventional and well known and is provided by the camera system of Nagai in at least paragraphs 32 and 37, where an image can be displayed or not and can be recorded in memory if desired. It would've been obvious to one having ordinary skill in the art at the time the invention was made to have the added feature of displaying or not while recording, since this can provide for saving power and also for

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selecting how the image is to be record as taught by Nagai.

For claim 11, the image sensing apparatus as claimed in claim 1, wherein the image sensing apparatus comprises an electronic still camera is not explicitly provided by Nagano, but Nagano provides for the conventional and well known items of a camera including the well known optical sensor and A/D converters and output thereof. Nagai provides for an electronic still camera in at least the abstract. Nagai can use the A/D converters of Nagano with the electronic still camera of Nagai and vice versa. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use A/D converters with an electronic still camera, since the A/D converters provide for two optional modes for the advantage of speed and high resolution, and because the camera has the advantage of features modes including a zoom function, previewing the image, and image enhancement functions including at least gamma correction and color balancing.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, and Nagai, 2001/0010561, as applied to claims 7, 9, 11, and 13 above, and in view of Kubo et al., 6,639,626.

For claim 8, the image sensing apparatus as claimed in claim 7, wherein the digital signal processing block performs color interpolation processing is not explicitly provided by Nagai, but color interpolation is very typically used in an image signal processing circuit in a digital camera, such as that of Nagai noted above, where Nagai

provides for "processing such as a gamma correction and color balance adjustment". Kubo provides for basically the same thing in a digital camera, but also clearly teaches color interpolation as well in at least Fig. 5, block 211a, Fig. 10, block 81, the last full paragraph in c. 13 and the paragraph bridging cols. 14-15, where the colors are RGB. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use color interpolation with at least the conventional and well known image signal processing of Nagai, since color interpolation is another conventional and well known image signal process, and because it and the other functions (gamma and color balancing) are common with Kubo and Nagai, and also provide for a higher fidelity image.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, and Nagai, 2001/0010561, as applied to claims 7, 9, 11, and 13 above.

For claim 10, the image sensing apparatus as claimed in claim 5, further comprising: an image storage block for storing the output signal from the digital signal processing block as image data; and an image display block for displaying the image according to the output signal from the digital signal processing block, wherein the solid state image sensing element, the AD conversion block, and the digital signal processing block stop operation while the image display block is displaying an image according to the image data stored in the image storage block, Nagai provides for storage from the DSP and displaying from the DSP, but does not explicitly recite stopping the operations.

However, since Nagai teaches playing back the images stored from memory (play back in paragraphs 45-50 and Fig. 5 as opposed to Fig. 4 picture taking mode), it inherently or clearly follows that the CCD, A/D converter, and DSP are not operating, since the image is not sensed unless in the picture taking mode and if the user presses the shutter-release in Fig. 4. Thus, if there is no image being sensed, then the CCD and all circuitry that come after it do not operate on a signal as claimed.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano, 5,687,003, and Hasegawa et al., 5,384,645, and Nagai, 2001/0010561, as applied to claims 7, 9-11, and 13 above, and in view of JP 11-261871, Yoshihiro, as cited in the IDS.

For claim 10, see the rejection of at least claim 10 above without respect to Yoshihiro. Since claim 10 above is reasoned logically, Yoshihiro clearly teaches the idea of stopping operations clearly by cutting power to them, which can be used with at least Nagai for cutting power in the different modes and use power where only power is necessary. See the abstract of Yoshihiro. It would've been obvious to one having ordinary skill in the art at the time the invention was made to cut power to some circuits, since only certain circuits are needed for display as taught by Yoshihiro, which provides for the advantage of saving power, which is very advantageous in small low power digital still cameras.

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano,

5,687,003, as applied to claims 1 and 4 above, and in view of Johnson et al., 6,686,957.

For claim 12, the image sensing apparatus as claimed in claim 1, wherein the A/D conversion block receives a bit count conversion signal from the image quality mode setting block, and converts the analog signal based on the bit count conversion signal can be considered provided by Nagano, since the data selector of Nagano in Fig. 1 can be considered part of the A/D conversion process. However, the A/D converters per se do not explicitly receive the quality mode. A/D converters per se receiving a quality mode is considered provided by Johnson in at least the first three full paragraphs in c. 8. Using the arrangement of Johnson can be used with the arrangement of Nagano by directly controlling the A/D converter, since either way – whether the A/D converters are directly controlled or not, Nagano would still provide for selecting a different bit count conversion as desired. It would've been obvious to one having ordinary skill in the art at the time the invention was made to control the A/D converter directly based on a quality mode setting signal as taught by Johnson with Nagano, since Johnson teaches at least “considerable power and battery savings” – same exact idea and purpose of Applicant.

15. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., 6,686,957, as applied to claims 14-17 and 24 above, and further in view of Hasegawa et al., 5,384,645.

For claim 18, see the rejection of at least claim 14, and the image sensing apparatus as claimed in claim 17, wherein the DSP block sets a corresponding

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quantization bit count when an image quality mode is set by the image quality mode setting block is almost implicit with Johnson, since Johnson explicitly provides for a DSP, and since such an image processor gets its input from the image sensing system, such system would operate in accordance with the quantization bit count set by Johnson, e.g. preview mode for displaying. In any case, Hasegawa explicitly teaches this in at least the second full paragraph in c. 3. Adapting the DSP, i.e. image processing, of Hasegawa with a different quantization bit count is exactly what Hasegawa teaches, and image processing is the next stage in the processing of Johnson, where Johnson outputs different quantization bit counts based on modes. Using a DSP for different quantization bit counts can be used with the DSP of Johnson. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use a DSP for different quantization bit counts, since Hasegawa provides for at least the advantages of a decrease in circuitry heat and therefore a reduction in power consumption as well, improvement in processing speed, and without changing memory to process image data.

16. Claims 19 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., 6,686,957, as applied to claims 14-17 and 24 above, and further in view of Nagai, 2001/0010561.

For claim 19, the image sensing apparatus as claimed in claim 17, further comprising a data thinning block for thinning the output signal from the digital signal

processing DSP block is not explicitly provided by Johnson, but is conventional and well known, and is provided by Nagai in at least paragraphs 25-26 on page 2, which is provided after or to the output of the digital signal processing as claimed. Thinning the output of the DSP of Nagai can be used at the output of the DSP of Johnson. It would've been obvious to one having ordinary skill in the art at the time the invention was made to thin the output of a DSP in processing with Johnson as taught by Nagai, since this provides for at least fast processing.

For claim 21, the image sensing apparatus as claimed in claim 17, further comprising: an image storage block for storing the output signal from the DSP block as image data is not explicitly provided by Johnson. Storing the output signal from the DSP block is conventional and well known and is provided by Nagai in at least paragraphs 32 and 37, where an image can be displayed or not and can be recorded in memory if desired, and the memory can store the output of the DSP of Johnson. It would've been obvious to one having ordinary skill in the art at the time the invention was made to have the added feature of displaying or not while recording, since this can provide for saving power and also for selecting how the image is to be recorded/stored as taught by Nagai.

For claims 22, the image sensing apparatus as claimed in claim 21, further comprising an image display for displaying the image according to the output signal from the DSP block is provided by Johnson by at least the display of Fig. 1. The image

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display block selecting whether to display the image during storage of the image data in the image storage block is not explicitly provided by Johnson, but is conventional and well known and is provided by the camera system of Nagai in at least paragraphs 32 and 37, where an image can be displayed or not and can be recorded in memory if desired, which can be used with the DSP and display of Johnson. It would've been obvious to one having ordinary skill in the art at the time the invention was made to have the added feature of displaying or not while recording, since this can provide for saving power and also for selecting how the image is to be record as taught by Nagai.

For claim 23, the image sensing apparatus as claimed in claim 17, further comprising: an image storage block for storing the output signal from the digital signal processing block as image data; and an image display block for displaying the image according to the output signal from the digital signal processing block, wherein the solid state image sensing element, the A/D conversion block, and the digital signal processing block stop operation during displaying by the image display block of an image based on image data stored in the image storage block is considered provided by Nagai, since Nagai provides for storage from the DSP and displaying from the DSP, but Nagai does not explicitly recite stopping the operations. However, since Nagai teaches playing back the images stored from memory (play back in paragraphs 45-50 and Fig. 5 as opposed to Fig. 4 picture taking mode), it inherently or clearly follows that the CCD, A/D converter, and DSP are not operating, since the image is not sensed unless in the picture taking mode and if the user presses the shutter-release in Fig. 4. Thus, if there

is no image being sensed, then the CCD and all circuitry that come after it do not operate on a signal as claimed, because there is no signal to operate on.

17. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., 6,686,957, Nagai, 2001/0010561, as applied to claims 19 and 21-23 above, and further in view of Kubo et al., 6,639,626.

For claim 20, the image sensing apparatus as claimed in claim 19, wherein the digital signal processing block performs color interpolation processing is not explicitly provided by Nagai or Johnson, but color interpolation is very typically used in an image signal processing circuit in a digital camera, such as that of Nagai noted above, where Nagai provides for "processing such as a gamma correction and color balance adjustment". Kubo provides for basically the same thing in a digital camera, but also clearly teaches color interpolation as well in at least Fig. 5, block 211a, Fig. 10, block 81, the last full paragraph in c. 13 and the paragraph bridging cols. 14-15, where the colors are RGB. Nagai and Johnson can use color interpolation with DSP, since this is a well known image processing. It would've been obvious to one having ordinary skill in the art at the time the invention was made to use color interpolation with at least the conventional and well known image signal processing of Nagai and Johnson, since color interpolation is another conventional and well known image signal process, and because it and the other functions (gamma and color balancing) are common with Kubo and Nagai, and also provide for a higher fidelity image.

18. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., 6,686,957, and Nagai, 2001/0010561, as applied to claims 19 and 21-23 above, and further in view of JP 11-261871, Yoshihiro, as cited in the IDS.

For claim 23, see the rejection of at least claim 23 above without respect to Yoshihiro. Since claim 23 above is reasoned logically without a reference, Yoshihiro is cited clearly teaching the idea of stopping operations by cutting power to them, which can be used with at least Nagai for cutting power in the different modes and use power where only power is necessary. See the abstract of Yoshihiro. It would've been obvious to one having ordinary skill in the art at the time the invention was made to cut power to some circuits, since only certain circuits are needed for display as taught by Yoshihiro, which provides for the advantage of saving power, which is very advantageous in small low power digital still cameras.

Response to Amendment

19. Applicant's arguments filed April 20, 2004 have been fully considered but they are not persuasive.

The Applicant argues on pages 14-18 of the amendment the following:

1. That because both A/D converters of Nagano operate continuously and because nothing controls the inputs or outputs of the two A/D converters, that Nagano does not provide for setting only one image quality mode and further does not provide for an A/D conversion block for converting to digital with a bit count corresponding only to the one image quality mode set.

2. That newly added independent claim 14 (Applicant recites claim 13 as independent; however, claim 13 is dependent) likewise distinguishes from the references.

The Examiner respectfully disagrees:

1. Nagano clearly provides for setting only one image quality setting mode, which is clearly shown in Fig. 1 supplied to a selector. Nagano provides for at least one A/D conversion block for converting to digital with a bit count corresponding only to the one image quality mode, since the image quality mode selects only one of the A/D converter outputs. Furthermore, the outputs of the A/D converters are clearly controlled by the data selector of Fig. 1 of Nagano, which is a critical feature of Nagano's invention.

2. Newly added independent claim 14 is not rejected based on previous references of record.

Final

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy M Johnson whose telephone number is 703-306-3096. The examiner can normally be reached on Monday – Friday from 5:30 to 2:00.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh M. Mehta, can be reached on Monday – Friday from 9:30 to 5:00. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Timothy M. Johnson
Patent Examiner
Art Unit 2625
May 23, 2004


TIMOTHY M. JOHNSON
PRIMARY EXAMINER